REMARKS

In response to the Advisory Action mailed on January 5, 2004 and the Notice of Appeal mailed February 3, 2004, claims 13, 32, 34, 36, 40, 42, 44, 48, 50 and 52 are amended and claims 56-60 are canceled without prejudice or disclaimer; as a result, claims 13-16 and 32-55 are now pending in this application.

This paper incorporates all of the previous arguments used in addressing the rejections. Applicant reserves the right to use the arguments in an appeal of the present application if appropriate.

Applicant maintains its right to swear behind the cited references in this rejection, and statements distinguishing the claimed subject matter over the cited documents are not to be interpreted as admissions that the documents are prior art.

§103 Rejection of the Claims

Claims 13-16 and 32-60 were rejected under 35 USC § 103(a) as being unpatentable over Katayama et al. (U.S. Patent No. 5,875,452) in view of Rosich et al. (U.S. Patent No. 5,587,964). Applicant respectfully traverses the rejections. Grounds for the traversal for the individual claims are stated below.

The Office Action states that the disclosure never supported this feature prior to the proposed Figure 6, stating that this feature is not new matter is equivalent to an admission that a DRAM containing its own row decoder, column decoder, data in buffer and data out buffer was prior art. Applicant makes no such admission. Applicant has never admitted that the proposed Figure 6 was prior art.

With Reference to claim 13

The office action mailed August 5, 2003 in section 3 especially directs attention to Katayama's figure 9, and states that the reference teaches a "unidirectional command and address bus" in the third paragraph of section 3, and then states in the fifth paragraph of section 3 (on page 3) that the reference teaches "bus 18 comprises, in part, a control bus and an address bus". Applicant respectfully submits that if bus 18 is to be identified as part of the command and

address bus, then the reference fails to disclose at least the feature of independent claim 13 of a unidirectional command and address bus, because bus 18 in Katayama's figure 9 and in Katayama's first embodiment shown in figure 2, is a bidirectional bus. This point is further supported by Katayama's discussion at least at column 16, lines 58-59. Further, Applicant can not see how either of the suggested command and address buses are directly connected to the first registers, such as items 131 figure 1 of Applicant's disclosure, and as required by independent claim 13.

The office action mailed August 5, 2003 uses the cited Rosich reference to show a memory device that is compatible with Katayama's memory controller that teaches the missing feature of Katayama of a data in buffer and a data out buffer in each of the plurality of storage arrays. Applicant respectfully submits that even if the suggested combination of references were allowable, the result of the combination still does not describe or suggest all of the combination of features of the present claimed invention. The suggested combination does not contain any teaching that might be seen as curing the deficiencies of the Katayama reference discussed above. In particular, the suggested combination still does not describe or suggest the combination of claimed features of a separate unidirectional command and address bus that is directly connected to each one of the command and address buffers found in the plurality of memory subsystems.

In view of the above noted failure of the suggested combination of references to describe or suggest at least the above noted combination of features of independent claim 13, Applicant respectfully requests that this rejection be withdrawn. Applicant respectfully requests reconsideration and allowance of claim 13.

Regarding claims 14 – 16:

If an independent claim is nonobvious under 35 U.S.C. § 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596(Fed. Cir. 1988).

Claims 14-16 depend on claim 13 and are believed to be allowable at least for the reasons stated previously for claim 13. Applicant respectfully requests reconsideration and allowance of claims 14-16.

Regarding claims 32 and 33:

Claim 32 was amended. Applicant is unable to find in the cited portions of the proposed combination of references, among other things, a teaching or suggestion of a method operating with wherein the socket couples the memory module to a separate unidirectional command and address bus and to a separate bidirectional data bus. Moreover, applicant can not find in the cited portions of the references the flowing features of claim 32 communicating commands and addresses, through the socket to the memory module, on the separate unidirectional command and address bus or communicating data, through the socket to the memory module, on the separate bidirectional data bus as recited in claim 32.

Claim 33 depends on claim 32 and is believed to be allowable at least for the reasons stated previously for claim 32. Applicant respectfully requests reconsideration and allowance of claims 32 and 33.

Claims 34 and 35:

Applicant is unable to find in the cited portions of the proposed combination of references, among other things, a teaching or suggestion of a method, operating with wherein the socket couples the memory module to a separate unidirectional command and address bus and a separate bidirectional data bus, including communicating commands and addresses, through the socket to the memory module, on the separate unidirectional command and address bus or communicating the data, through the socket to a memory controller, on the separate bidirectional data bus.

Claim 35 depends on claim 34 and is believed to be allowable at least for the reasons stated previously for claim 34. Applicant respectfully requests reconsideration and allowance of claims 34 and 35.

Claims 36-39:

Applicant believes that claim 36 is allowable for substantially similar reasons as claim 13. More specifically, applicant is unable to find in the cited portions of the proposed

combination of references, among other things, a teaching or suggestion of a memory module having a connector, wherein the connector includes unidirectional command and address lines coupled to the first register and bidirectional data lines coupled to the data register, wherein the connector is capable of being connected through a socket to a separate unidirectional command and address bus and a separate bidirectional data bus, wherein the separate bidirectional data bus is directly connected to the data buffer. Instead, Applicant believes the proposed combination of references teach or suggest external data buffers in common use by the memory devices. Claims 37-39 depend on claim 36 and are believed to be allowable at least for the reasons stated previously for claim 36. Applicant respectfully requests reconsideration and allowance of claims 36-39.

Claims 40 and 41:

Applicant is unable to find in the proposed combination of references, among other things, a teaching or suggestion of a method that operates with wherein the bidirectional data bus being separate from the unidirectional command and address bus. Moreover, applicant can not find the following features in the cited portions of the applied documents: receiving commands and addresses, through the command and address lines separate from the bidirectional data lines, from the unidirectional command and address bus, the commands and addresses communicated according to a packet protocol or receiving data, through the data lines, from the data bus separate from the command and address lines, the data communicated according to a packet protocol, as recited in claim 40.

Claim 41 depends on claim 40 and is believed to be allowable at least for the reasons stated previously for claim 40. Applicant respectfully requests reconsideration and allowance of claims 40 and 41.

Regarding claim 42 and 43:

Applicant is unable to find in the cited portions of the proposed combination of references, among other things, a teaching or suggestion of a method including wherein the connector is capable of being connected through a socket to a separate unidirectional command

and address bus and a separate data bus, receiving commands and addresses, through the command and address lines, from the separate unidirectional command and address bus or communicating the data from the data register, through the data lines, to the separate data bus, as recited in claim 42.

Claim 43 depends on claim 42 and is believed to be allowable at least for the reasons stated previously for claim 42. Applicant respectfully requests reconsideration and allowance of claims 42 and 43.

Claims 44-47:

Applicant is unable to find in the cited portions of the proposed combination of references, among other things, a teaching or suggestion of a separate unidirectional command and address bus coupled to the memory controller, the memory controller communicating commands and addresses to the separate unidirectional command and address bus or a separate bidirectional data bus coupled to the memory controller, the memory controller communicating data information to the bidirectional data bus for a write operation and receiving the data information from the bidirectional data bus during a read operation, as recited in claim 44. Applicant further can not find the following features of claim 44 in the cited portions of the applied documents a plurality M of memory devices, wherein each memory device contains a data in and a data out buffer directly connected to the separate bidirectional data bus; a first register connected between the separate unidirectional command and address bus and the plurality of memory devices, the first register receiving and latching the commands and addresses from the command and address bus and driving the commands and addresses to the plurality of memory devices; and a data register directly connected between the plurality of memory devices and the separate bidirectional data bus.

Claims 45-47 depend on base claim 44. Applicant believes claims 45-47 are allowable at least for the reasons stated previously for claim 44. Applicant respectfully requests reconsideration and allowance of claims 44 – 47.

Claims 48 -51:

Applicant is unable to find in the cited portions of the proposed combination of references, among other things, a teaching or suggestion of a method including the socket couples the memory module to a separate unidirectional command and address bus and a separate bidirectional data bus, communicating information to the memory controller, wherein the memory controller receives the information and wherein the memory controller issues commands and addresses to the separate unidirectional command and address bus, communicating the commands and addresses from the separate unidirectional command and address bus, through the socket, to the memory module; communicating data from the memory controller to the separate bidirectional data bus; communicating the data from the separate bidirectional data bus to the memory module, as recited in claim 48.

Claim 49 depends on base claim 48. Applicant believes that claim 49 is allowable at least for the reasons stated previously for claim 48.

Applicant respectfully requests reconsideration and allowance of claims 48-49.

Claims 50 and 51:

Applicant asserts that claims 50 and 51 are allowable at least for substantially similar reasons as stated above with regard to claim 49. Allowance of claims 50-51 is requested.

Claims 52-55:

Applicant asserts that claim 52 is allowable at least for substantially similar reasons as stated above with regard to claim 44. Claims 53-55 depend from claim 52 and are believed to be allowable therewith. Allowance of claims 52-55 is requested.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 349-9587 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Amy Moriarty
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Signature

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